REMARKS

Claims 1-13 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Peter Scott at (719)533-7969 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 103

Claims 1, 2, 7, 8, 12 and 13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Si et al., U.S. Patent No. 4,819,166 (*Si*) in view of Cliff et al., U.S. Patent No. 6,023,439 (*Cliff*) and Tomita, U.S. Patent No. 6,442,092 B1 (*Tomita*). Applicant respectfully traverses the rejection as follows.

Regarding Claim 1, the rejection proposes on pages 2-3 to modify *Si* to include the RAM block (447) and the column decoder (448) of FIG. 21B in *Cliff*. However, the rejection fails to establish how the RAM block (447) and the column decoder (448) in *Cliff* teaches or suggests the input data register and the input buffer recited in Claim 1. If the rejection is not withdrawn, Applicant requests that the alleged relevance of the RAM block (447) and the column decoder (448) in *Cliff* to the claimed elements be clearly explained. Further, the rejection fails to provide a reasonable explanation of how the proposed modification to *Si* by *Cliff* might be made, that is, specifically how the RAM block (447) and the column decoder (448) may be connected in FIGS. 2 and 6 of *Si* as proposed by the rejection. Absent such

an explanation, the proposed modification lacks sufficient support to sustain the rejection of Claim 1 under 35 U.S.C. § 103.

Further, the rejection alleges on page 3 that *Tomita* discloses the claimed latch bypass multiplexer in column 8, lines 45-52 and that it would be obvious to modify *Si* and *Cliff* by *Tomita* to arrive at the invention recited in Claim 1. In column 8, lines 45-52 cited by the rejection, *Tomita* explains that the multiplexer (70) selects one of four different types of signals: the scan output signals from the instruction register 62, the bypass register 64, the scan number register 66, and the multiplexer output signal S8.

In contrast to *Tomita*, the claimed latch bypass multiplexer selects either the input data buffer or the latch array to generate either a first data output of the latch based random access memory from the input data buffer during logic scan testing or a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal. Clearly, the rejection fails to show that the multiplexer (70) in *Tomita* teaches or suggests selecting a data output from one of the claimed input data buffer and the claimed latch array. Because the rejection cites a reference that teaches a multiplexer that performs a different function than the claimed function, the rejection fails to arrive at the claimed invention. Further, the rejection fails to show that *Tomita* teaches or suggests that the multiplexer (70) responds to a memory scan mode signal. Because the multiplexer (70) in *Tomita* does not teach or suggest selecting one of the input data buffer and the latch array to generate a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output

of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal, the modification of *Si* and *Cliff* by *Tomita* proposed by the rejection fails to arrive at the claimed invention recited in Claim 1. Because the modification proposed by the rejection fails to arrive at the claimed invention, Claim 1 is not obvious under 35 U.S.C. § 103(a).

Even if the modification proposed by the rejection would work, the argument made in the rejection for motivation to make the proposed modification is invalid, because the rejection assumes what the argument is supposed to prove. Specifically, the rejection states on page 3 that "...one of ordinary skill in the art would have recognized that it would provide the opportunity to selectively conduct logic scan testing and memory scan testing". Not only is the reasoning circular, but also it is clearly based solely on hindsight gained from Applicant's disclosure. See, for example, the paragraph beginning on page 16, line 25 of the specification: "An important aspect of the present invention is that instead of testing all the logic functions of the die in one scan test, the scan test is partitioned into a logic scan test and a memory scan test to reduce the total test time required of the automated test equipment (ATE) and to ensure complete fault coverage of both the LBRAMs and the surrounding logic in the integrated circuit die."

Because the rejection fails to make a valid argument to show motivation for making the proposed modification, and because the rejection relies solely on hindsight gained from Applicant's disclosure to show motivation for making the proposed modification, and because the proposed modification of *Si* and *Cliff* by *Tomita* fails to arrive at the claimed invention, Claim 1 is not obvious under 35 U.S.C. § 103(a).

Regarding Claim 2, the rejection alleges on page 4 that *Tomita* teaches the additional limitations of the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal. However, in FIGS. 6, 12 and column 8, lines 15-20 and column 10, lines 48-65 cited by the rejection, *Tomita* makes no mention of the claimed read address register, no mention of the claimed read address multiplexer, and no mention of the claimed selection of one of a logic scan address and a memory scan address in response to the memory scan mode signal. Because the rejection fails to show that all the limitations of Claim 2 are taught or suggested in *Tomita*, the rejection fails to arrive at the claimed invention. Because *Tomita* does not teach or suggest the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal, the modification of *Si* and *Cliff* by *Tomita* proposed by the rejection lacks sufficient support to sustain a rejection of Claim 2 under 35 U.S.C. § 103.

Further, even if *Tomita* did teach or suggest the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal, the rejection fails to provide a reasonable explanation of how the proposed modification might be made, that is, how the elements in *Tomita* would be connected in *Si* and *Cliff* to arrive at the claimed invention. Absent such an explanation, the proposed modification lacks sufficient support to sustain the rejection

of Claim 2 under 35 U.S.C. § 103.

Regarding Claim 7, the rejection alleges that *Tomita* teaches the claimed method of:

(a) modifying a latch based memory to include a latch array bypass multiplexer for selecting one of an input data buffer of the latch based random access memory and a latch array of the latch based random access memory for generating a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal;

(b) asserting the memory scan mode signal during a memory scan test; and

(c) removing the memory scan mode signal during a logic scan test.

However, in FIGS. 6, 12 and column 8, lines 15-20 and column 10, line 48 to column 11, line 14 cited by the rejection, *Tomita* makes no mention of step (a), no mention of step (b), and no mention of step (c) recited in Claim 7. If the rejection is not withdrawn, Applicant requests that the rejection show specifically and clearly where each of the claimed steps recited in Claim 7 is taught or suggested in *Tomita*.

Regarding Claim 8, the rejection alleges on page 4 that *Tomita* teaches selecting one of a logic scan address and a memory scan address for coupling to a read address register of the latch based random access memory in response to the memory scan mode signal. However, in column 10, lines 48-65 cited by the rejection, *Tomita* makes no mention of the claimed

logic scan address, no mention of the claimed memory scan address, and no mention of coupling one of them to a read address register of the latch based random access memory in response to the memory scan mode signal. If the rejection is not withdrawn, Applicant requests that the rejection show specifically and clearly where *Tomita* teaches or suggests each of the claimed logic scan address, the claimed memory scan address, and coupling one of them to a read address register of the latch based random access memory in response to the memory scan mode signal as recited in Claim 8.

Regarding Claim 12, the rejection alleges on page 4 that *Tomita* teaches the claimed step of bypassing logic chains surrounding the latch based random access memory during a memory scan test. However, in FIG. 6 and column 8, lines 45-52 and column 10, line 66 to column 11, line 14 cited by the rejection, *Tomita* makes no mention of bypassing logic chains surrounding the latch based random access memory during a memory scan test. If the rejection is not withdrawn, Applicant requests that the rejection show specifically and clearly where *Tomita* teaches or suggests bypassing logic chains surrounding the latch based random access memory during a memory scan test as recited in Claim 12.

Regarding Claim 13, the rejection alleges on page 4 that *Tomita* teaches the additional limitation of bypassing the latch array during a logic scan test. However, in column 8, lines 14-19 and 45-52 cited by the rejection, *Tomita* makes no mention of bypassing the latch array during a logic scan test. If the rejection is not withdrawn, Applicant requests that the rejection show specifically and clearly where *Tomita* teaches or suggests bypassing the latch array during a logic scan test

as recited in Claim 13.

Claims 3 and 9 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Si*, *Cliff*, and *Tomita* as applied to Claim 2 and further in view of Lach, et al., U.S. Patent No. 5,909,451 (*Lach*). The rejection of Claims 3 and 9 is traversed for the same reasons as the rejection of Claims 1, 2, 7 and 8.

Claims 4 and 10 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Si*, *Cliff*, *Tomita*, and *Lach* as applied to Claim 3, and further in view of Sindhu, U.S. Patent No. 5,123,101 (*Sindhu*). Applicant respectfully traverses the rejection as follows.

Regarding Claims 4 and 10, the rejection alleges on page 6 that *Sindhu* discloses the claimed bypass logic for controlling the latch array bypass multiplexer in response to the memory scan mode signal and the scan mode signal in FIG. 4 and column 16, lines 47-51. However, as may easily be seen in *Sindhu*'s FIG. 4, the bypass multiplexer (138) does not perform the same functions as the claimed latch bypass multiplexer recited in Claims 1 and 7. In column 16, lines 47-51 cited by the rejection, *Sindhu* makes no mention of selecting one of the input data buffer and the latch array to generate a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal. Because *Sindhu*'s bypass multiplexer (138) does not perform the same functions as the claimed latch bypass multiplexer, the bypass logic (136) for the bypass multiplexer (138) would not work in the modification proposed by the

rejection to arrive at the claimed invention, even if the rejection provided a reasonable explanation of how the proposed modification might be made from the five disparate devices required by the rejection. Because the bypass logic (136) would not work in the modification proposed by the rejection to arrive at the claimed invention, and because the rejection fails to provide a reasonable explanation of how the proposed modification might be made, the proposed modification lacks sufficient support to sustain a rejection of Claims 4 and 10 under 35 U.S.C. § 103.

The rejection of Claims 5, 6 and 11 is traversed for the same reasons as the rejection of Claims 1, 2, 3 and 7.

No additional fee is believed due for this response.

Respectfully submitted,

/ Eric James Whitesell /

Eric James Whitesell #38,657

Address all correspondence to:
LSI Logic Corporation
1621 Barber Lane, M/S D-106
Milpitas, CA 95035-7458

Direct telephone inquiries to:
Peter Scott
(719) 533-7969